What is Claimed is:

1. A phase-locked loop, comprising:

a divider for receiving a reference clock with a substantially fixed period and generating an output clock with a time-varying period;

a noise-shaped quantizer for quantizing a period control word to a time-varying value in response to said output clock fed from said divider so that said divider generates said output clock by means of dividing said reference clock by said time-varying value;

a filter for substantially filtering out jitter from said output clock;

a phase detector for generating a phase error in response to said filtered output clock and an input signal; and

a digital loop filter for generating said period control word in response to said phase error.

2. The phase-locked loop as claimed in claim 1, wherein said period control word has a bit resolution greater than that of said time-varying value.

3. The phase-locked loop as claimed in claim 1, wherein said noise-shaped quantizer is a delta-sigma quantizer.

4. The phase-locked loop as claimed in claim 1, wherein said filter is an analog phase locked loop (PLL) device as a low pass filter for removing high frequency jitter from said output clock.

5. The phase-locked loop as claimed in claim 1, further comprising a phase

shifter for shifting a phase of said filtered output clock.

6. The phase-locked loop as claimed in claim 1, further comprising another divider for dividing said filtered output clock by a divisor such that said phase detector generates said phase error in response to said divided output clock and said input signal.

7. A phase-locked loop, comprising:

a first divider for receiving a reference clock with a substantially fixed period and generating an output clock with a time-varying period;

a noise-shaped quantizer for quantizing a period control word to a time-varying value in response to said output clock fed from said first divider so that said first divider generates said output clock by means of dividing said reference clock by said time-varying value;

a filter for substantially filtering out jitter from said output clock;

a second divider for dividing said filtered output clock by said period control word so as to generate one divided output clock;

a phase detector for generating a phase error in response to said divided output clock and an input signal; and

a digital loop filter for generating said period control word in response to said phase error.

8. The phase-locked loop as claimed in claim 7, wherein said period control word has a bit resolution greater than that of said time-varying value.

9. The phase-locked loop as claimed in claim 7, wherein said noise-shaped

quantizer is a delta-sigma quantizer.

10. The phase-locked loop as claimed in claim 7, wherein said filter is an analog phase locked loop (PLL) device as a low pass filter for removing high frequency jitter from said output clock.

11. The phase-locked loop as claimed in claim 7, further comprising a phase shifter for shifting a phase of said filtered output clock.

12. The phase-locked loop as claimed in claim 7, further comprising a third divider for dividing said one divided output clock by a divisor to another divided output clock such that said phase detector generates said phase error in response to said another divided output clock and said input signal.